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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,468	12/26/2000	Naoki Tsuji	49657-862	1840

7590 09/18/2003

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,468	TSUJI, NAOKI	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2 and 4,11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' request for reconsideration has been entered.

As applicants' have shown in the request for reconsideration the previously applied Kawashima et al. (6,153,918) reference has a publication date of November 28, 2000 and the instant Application has an effective filing date July 24, 2000 the U.S. 6,153, 918 cannot be a valid reference because the statement of common ownership in the request for reconsideration.

However, US 6,153, 918 itself claims priority from Japanese Patent Publication No. 2000-227211 (Application No. 10-109535) which was published on January 14, 2000 well before the earliest effective filling date of the instant application (July 24, 200O) . This Japanese Patent Publication is available as a 102(a) reference also and therefore the provisions of the 35 U.S.C. 103 (c) are not applicable to the priority Japanese Patent Publication No. 2000-227211 (Application No. 10-109535).

The enclosed Final rejection substitutes the Final rejection mailed on March 17, 2003.

Therefore Claim1 as amended by the amendment and claims 2 and 11 as recited in the amendment of May 21,2202 and claim 4 as originally recited are currently pending in the application.

Election/Restrictions

This application contains claims 5 to 10 drawn to an invention nonelected without traverse in Paper No.4. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent No. 5,946,230 , herein after Shimizu) previously applied and in view of Kawashima et al. (Japanese Patent Publication No. 2000-227211 which is the priority document for U.S. 6,153,918, herein after Kawashima) newly applied.

With respect to claim 1, Shimizu describes substantially all the limitations presently recited in the claim as previously stated reproduced below for ready reference.

With respect to claim 1, Shimizu describes a Nonvolatile semiconductor memory device including - a first region having first transistors having a first gate oxide thickness (Shimizu Abstract line 1 memory cell array section, and line 13 for first thickness),- a second region with second transistors with a second gate oxide thickness (Abstract line 2 peripheral driving circuit section and thickness line 114); trench isolation regions

formed selectively within first and second regions (e.g. Fig. 21 B # 12 STI) -1 a dummy region having plurality of dummy STI located between first and second regions (figs. 24 and 25); a positioning mark (DPC) formed between the plurality of dummy trench isolation regions and is used to position the mask film (Shimizu fig. 13 A and B and col. 13 line 63- col. 14 lines 14).

Shimizu does not specifically state the dummy pattern cell (DPC) as being the positioning mark of the dummy pattern region, however it is inherent from the way the IDPC is used for e.g. col.12 lines 21-25 that the DPC is used as a positioning mark to form different pattern cells in the different regions.

The other limitations of claim 1 are :

a second region adjacent to the first region (Shimizu fig. 13b etc.)

Trench isolation patterns (Shimizu fig. 21 b # 12 (STI), and extending continuously in a first direction (Shimizu Fig. 21 B #12 extending continuously in at least the lateral and/or vertical directions) .

A dummy isolation region (Shimizu fig.13 B) having the dummy trench isolation patterns comprise a patterns, which constitutes a positioning mark and extends in a second direction different from the first direction. (Shimizu figs. 13B to 15 reproduced below , col. 13 line 63 to col. 14 lines 14 and col.22 line 45-60).

Shimizu does not specifically mention the presently newly added limitation " so as to connect said dummy trench isolation patterns."

However, Kawashima in the figure 5 , etc. shows the dummy trench isolation patterns 3 being connected by layer 20a (figure 5) so that the junction surfaces and the dummy region can be surfaces having different impurity concentrations but of the same conductivity type.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Kawashima's connection so as to connect said dummy trench isolation patterns in Shimizu's device. The motivation to combine the references as stated above is at least to provide the junction surfaces and the dummy region can be surfaces having different impurity concentrations but have the same conductivity type. (Kawashima- English Abstract title section).

With respect to claim 2, the semiconductor device including memory cell region Shimizu Abstract line 1) and peripheral circuit region controlling the memory cell transistors(Shimizu Abstract line 2 and last 3 lines) wherein the first and second regions "(i.e. the memory cell region and the peripheral circuit region) "are arranged in the first direction " (Shimizu see figs. 13 B to 15 above) "and the dummy region extends in the first direction along the first and second regions." (see above Shimizu figures the dummy region extends in the first direction (i.e. parallel to the substrate) along the memory region (first region) and peripheral (second region) i.e. region at the extreme left of the figure that is not marked but clearly identified in Shimizu figs. 5, 12A, 21 A etc.).

With respect to claim 3 wherein the semiconductor memory device is a non-volatile semiconductor memory device (Shimizu title).

With respect to claim 4, wherein the positioning mark includes a trench part formed to connect dummy trench isolation regions. (Shimizu fig. 12 metal wirings WL1 And WIL2 connected to row decoder section through DPC).

With respect to claim 11, to the extent understood, Shimizu describes a semiconductor device wherein the pattern of the dummy trench isolation extends in a vertical direction with respect to the first direction. (See fig. 21 b # 12 (STI), reproduced below and extending in vertical direction) .

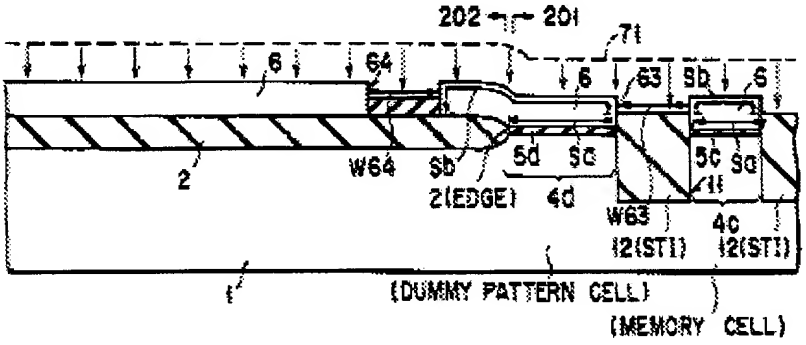

FIG. 21B

Response to Arguments

Applicant's arguments with respect to claims 1,2,4 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

September 17, 2003.

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800